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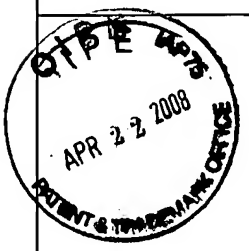
PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)
JAR-1035-473



Application Number	Filed
10/668,166	September 24, 2003
First Named Inventor	
KIMURA	
Art Unit	**Examiner**
2811	ARENA, Andrew O.

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

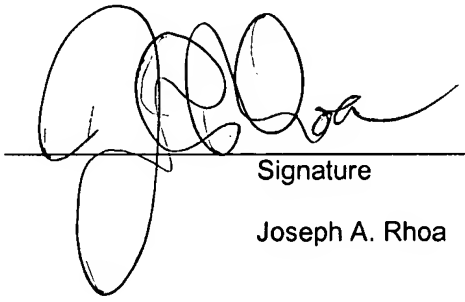
I am the

☐ Applicant/Inventor

☐ Assignee of record of the entire interest. See 37 C.F.R. § 3.71. Statement under 37 C.F.R. § 3.73(b) is enclosed. (Form PTO/SB/96)

☒ Attorney or agent of record 37,515 (Reg. No.)

☐ Attorney or agent acting under 37CFR 1.34.
Registration number if acting under 37 C.F.R. § 1,34 _____



Signature

Joseph A. Rhoa

Typed or printed name

703-816-4043

Requester's telephone number

April 22, 2008

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.*

☒ *Total of 1 form/s are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

KIMURA et al. Atty. Ref.: 1035-473; Confirmation No. 4031

Appl. No. 10/668,166 TC/A.U. 2811

Filed: September 24, 2003 Examiner: ARENA, Andrew O.

For: SEMICONDUCTOR DEVICE AND CHIP-STACK SEMICONDUCTOR DEVICE

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April 22, 2008

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Pursuant to the OG Notice of July 12, 2005, applicant hereby requests a pre-appeal brief review of this case for at least the following reasons.

Claim 1 stands rejected under Section 103(a) as being allegedly unpatentable over Sumikawa (US 6,362,529) in view of Anderson (US 6,661,100). This Section 103(a) rejection is respectfully traversed.

Claim 1 requires "at least two of the plurality of through electrodes are connected to one another to form a first high-current through electrode that is in communication with a power supply, at least another two of the plurality of through electrodes are connected to one another to form a second high-current through electrode that is in communication with ground . . . at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any

electrode pad of the chip." In other words, at least one of the through electrodes "electrically link[s]" the front surface of the chip to the back surface of the chip and is a "*non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip.*" For example and without limitation, see the right-hand non-contact through electrode 19 in Fig. 3 of the instant application which is electrically isolated from the chip; and non-contact through electrodes 19 in Figs. 8-9. See also pg. 17, lines 11-12, of the instant specification.

The cited art fails to disclose or suggest the aforesaid underlined and quoted feature of claim 1. In particular, both Sumikawa and Anderson fail to disclose or suggest a non-contact through electrode electrically linking the front surface of the chip to the back surface of the chip which is a "*non-contact through electrode which is electrically isolated from the chip so that said least one through electrode is not electrically connected to any electrode pad of the chip*" as required by claim 1. The Examiner relies on col. 4, lines 3-6 and 45-55 of Sumikawa for this feature. However, this portion of Sumikawa does not disclose or suggest such a non-contact through electrode. Instead, Sumikawa makes very clear that both penetrating electrodes (22a, 22b, 2a, 2b) are electrically connected to wiring patterns of the chip and transmit signals, thereby teaching directly away from the non-contact requirement of claim 1 (e.g., see Sumikawa from col. 4, line 60 to col. 5, line 6). Sumikawa's penetrating electrode 2 (see Fig. 3) and the penetrating electrodes 22a, 22b, 2a and 2b are electrically connected to electrode pads 7 of the chip and are also connected to wiring patterns 5a – the opposite of what claim 1 requires. Thus, even the alleged combination (which applicant believes would be incorrect in any event) fails to meet the above requirements of claim 1.

Claim 7 requires that "at least one of the through electrodes is a non-contact through type electrode which is not electrically connected to the semiconductor chip in which it is formed so that said least one through electrode is not electrically connected to any electrode pad of the chip" and claim 8 requires that "at least one of the through electrodes is a non-contact through electrode which is not electrically connected to any electrode pad of the chip in which it is formed." As explained above, the cited art fails to disclose or suggest each of these features of claims 7 and 8, respectively, either taken alone or in combination.

In response to applicant's arguments filed November 1, 2007, the Office Action dated January 28, 2008 contends that Fig. 4 of Sumikawa shows through electrode 22b not connected to any electrode pad. This allegation by the Examiner is incorrect. Sumikawa from col. 4, line 66 to col. 5, line 6, makes very clear that through electrode 2b and 22b are active electrodes. The electrodes 22a, 22b, 2a and 2b in Fig. 4 of Sumikawa are all electrically connected to members corresponding to electrode pads 7. In contrast, claim 1 requires that a through electrode is a non-contact through electrode which is *electrically isolated from the chip so that it is not electrically connected to any electrode pad.* Because, as explained by Sumikawa, electrode 22b is part of an active circuit, it cannot meet this requirement of claim 1.

Furthermore, regarding claims 9, 11, 12, 13, 15-17, 19 and 20, the Office Action has used impermissible hindsight reasoning to arrive at the claimed inventions. The Office Action asserts that it is well known that a larger total cross section is used for a longer conduction path to reduce impedance. The Office Action then asserts that one skilled in the art would connect through electrodes in order to reduce impedance. This latter assertion is certainly based on impermissible hindsight reasoning. Anderson teaches reducing impedance by using a wide, thick wire at col. 3, lines 57-64. Assuming arguendo for the sake of argument only that one were to

combine Anderson and Sumikawa, one skilled in the art wishing to reduce impedance would apply the teaching of Anderson and provide wider, thicker metal plugs. However, the pending claims call for through electrodes with substantially equal cross-sectional area, so this modification would not meet the pending claims. Moreover, Anderson teaches connecting a plurality of solder bumps in order to provide GND and VDD to various parts of the chips, the connection of multiple solder bumps in Anderson is entirely unrelated to reducing impedance; impedance is reduced in Anderson by using wide, thick wires. Thus, the rationale alleged by the Examiner for the combination lacks merit and is fundamentally flawed. Stated another way, one of ordinary skill in the art would not have made the modification alleged by the Examiner in order to reduce impedance as alleged by the Office Action; instead, one would have reduced impedance by using wide, thick wires as taught by Anderson which would not result in the claimed inventions recited in these claims.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance.

Respectfully submitted,

NIXON & VANDERHYE P.C.

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